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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,597	02/25/2005	Nevio Benvenuto	IT02 0025 US	3611

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EXAMINER	
NEFF, MICHAEL R	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,597	BENVENUTO ET AL.	
	Examiner	Art Unit	
	MICHAEL R. NEFF	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 10 of remarks, filed 4/10/2008, with respect to the rejection(s) of claim(s) 1 and 18 under Berberidis have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Crespo.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.,* 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-10, 18-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis et al. (herein after Berberidis) (US Patent 6,052,702, see IDS) in view of Crespo (US Patent 5,020,078).

Re Claims 1 and 18, Berberidis discloses a frequency-domain decision feedback equalizer device for single carrier modulation, preferably for use in a broadband

communication system, including a first section comprising: a fast Fourier transforming means (11) for performing a fast Fourier transformation on a first vector of signals (M, output from 10) inputted into said first section, and outputting a second vector of signals (2M), a feed forward equalization means for performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters (12 and the associated inputs to element 12), and outputting a third vector of signals (output from element 12), and an inverse fast Fourier transforming means (13) for performing an inverse fast Fourier transformation on said third vector of signals, and outputting a fourth vector of signals (M, output from 13); while Berberidis discloses a second section comprising a feedback equalizer structure, the disclosure fails to explicitly disclose the feedback equalizer design wherein a second section comprising: a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section, an adding means for adding the output signal of said feedback filter means to the output signal of said first section, and a detector means for receiving the output signal of said adding means and generating said output signal of said second section by extracting samples from the output signal of said adding means.

This design is however disclosed by Crespo. Crespo discloses a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section (33), an adding means for adding the output signal of said feedback filter means to the output signal of said first section (22), and a detector means for receiving the output signal of said adding means and generating said output signal of

said second section by extracting samples from the output signal of said adding means (23; Col. 3 line 35-Col. 4 line 2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feed back equalizer design as disclosed by Crespo to modify the feedback equalizer design of Berberidis in order to gain the benefit of a dynamic and self corrective means of producing correct estimated symbols from the detector output directly.

Re Claims 2 and 19, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18, Berberidis further discloses wherein said feed forward equalization means is provided for generating equalization parameters adapted for minimizing the signal-to-noise ratio of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section (FF, Col. 2 line 66-Col. 3 line 4; Col. 7 lines 42-55).

Re Claims 3 and 20, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18, while Berberidis discloses the feed forward equalization branch comprising Fourier functionality (FF), wherein said feed forward equalization means is provided for generating equalization parameters by taking into account a fast Fourier transformation estimation of a signal (Col. 5 lines 64-Col. 6 line 8; FF block and inclusive FFT and multiplier components); Crespo further discloses wherein the signal is the channel impulse response of the signal processed in

the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section (Col. 3 line 34-Col. 4 line 2).

Re Claims 4 and 21, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said first section further comprises: a serial to parallel converting means for converting a sequence of signals inputted into said first section to said first vector of signals (10, performs serial to parallel conversion of inputted signal [pre first section S/P manipulation]), and a parallel to serial converting means for converting said fourth vector of signals to a sequence of output signals of said first section (the M/PL element provides the ability to convert from parallel to serial; Col. 5 line 59-Col. 6 line 49 [post first section P/S conversion]).

Re Claims 5 and 22, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said serial to parallel converting means is adapted to receive scalar signals (1, 10, x(n); Col.1 lines 31-44; Col. 2 lines 38-65; Col. 5 line 59-Col. 6 line 8).

Re Claims 6 and 23, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said signal to parallel converting means is provided to generate said first vector

of signals including blocks of a predetermined number (P) of consecutive samples of the signals inputted into said first section (Col. 5 lines 60-67).

Re Claims 7 and 24, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said parallel to serial converting means and said feedback filter means are provided to output scalar signals (M/PL, y(n); Col. 2 lines 38-65, Col. 6 line 35-Col. 7 line 37).

Re Claims 8 and 25, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 6 and 23; Berberidis further discloses wherein said parallel to serial converting means is provided to output a scalar signal (Y) which is constituted by consecutive blocks of a predetermined number (M) of samples, each block being built with the predetermined number (M) of samples of each block of said fourth vector of signals (Abstract; Col. 5 line 59-Col. 6 line 63; further Col. 6 line 64-Col. 7 line 6).

Re Claims 9 and 26, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said detector means is adapted to receive and output discrete time signals (Col. 1 lines 5-67, Col. 6 line 64-Col. 7 line 37; Claim 3).

Re Claims 10 and 27, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said detector means is provided to generate said output signal (DO, y(n); Col. 5 line 59-Col. 6 line 63).

5. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Crespo as applied to claim 1 and 18 above, and further in view of Johnson et al. (herein after Johnson) (US Patent 5,808,574).

Re Claims 11 and 28, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said second section further comprises a feedback input generator means for receiving said output signal of said second section and providing an output signal which is built by consecutive blocks, each block comprising a predetermined number (M) of samples from said output signal of said section, to said feedback filter means (Abstract; Col. 5 line 59-Col. 6 line 63; further Col. 6 line 64-Col. 7 line 6); however Berberidis fails to explicitly disclose wherein each block is also including a pseudo noise sequence.

This design is however disclosed by Johnson. Johnson discloses a feedback system within a communication system wherein the signals within the feedback loop are adjusted to include a pseudo noise sequence (Col. 45 lines 29-43).

Therefore it would have been obvious to one of ordinary skill in the art a the time the invention was made to modify the feedback equalizer disclosure of Berberidis to

insert pseudo noise into the feedback signal as disclosed by Johnson in order to gain the benefit of improving on system performance and symbol detection.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Crespo as applied in claim 1 above, and further in view of Gay-Bellile et al. (herein after Gay) (US Publication 2002/0070796 A1).

Re Claim 12, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claim 1; Berberidis further discloses, wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device according to claim 1 (see rejection for claim 1 above); however the disclosure fails to explicitly disclose using a single carrier modulation within the equalizer.

However this system design is disclosed by Gay. Gay discloses a feedback equalizer device wherein single carrier modulation is used (Paragraphs0016, 20, 24-26).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of single carrier modulation within the feedback equalizer system as disclosed by Gay with the feedback equalizer disclosure of Berberidis in order to gain the benefit of having a system that can perform with lower power consumption than that of a system using multi-carrier modulation.

7. **Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Gay as applied in claim 1, and further in view of Thomas et al. (herein after Thomas) (US Publication 2004/0013084 A1).**

Re Claim 17, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claim 1; Berberidis further discloses a communication system including a transmitter for transmitting data, comprising a modulating means for organizing the data in blocks a receiver of a communication system, wherein said receiver includes a frequency-domain decision feedback equalizer device (see rejection of claim 1 above); however Berberidis fails to explicitly disclose wherein (1) the communication system is using a single carrier modulation, and although the use of a header on a data signal is well known to those of ordinary skill in the art, Berberidis does not explicitly disclose (2) wherein each block is separated by a sequence of a predetermined signal.

Regarding item (1) above, this system design is disclosed by Gay. Gay discloses a feedback equalizer device wherein single carrier modulation is used (Paragraphs0016, 20, 24-26).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of single carrier modulation within the feedback equalizer system as disclosed by Gay with the feedback equalizer disclosure of Berberidis in order to gain the benefit of having a system that can perform with lower power consumption than that of a system using multi-carrier modulation.

Regarding item (2) above, separating each data block by a sequence of a predetermined signal, or a signal header, is explicitly disclosed by Thomas (Fig. 1-5).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate separating the data symbol blocks by a predetermined header symbol as disclosed by Thomas with the feedback equalizer as disclosed by Berberidis in order to gain the benefit of improved symbol recognition and demodulating within the receiver end of the communication system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL R. NEFF whose telephone number is (571)270-1848. The examiner can normally be reached on Monday - Friday 8:00am - 4:30pm EST ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571)272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL R. NEFF/
Examiner, Art Unit 2611
/Shuwang Liu/
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